XILINX ALL PROGRAMMABLE

Defense-Grade UltraScale FPGA Data Sheet: Overview

DS895 (v1.0) January 31, 2017 **Product Specification**

General Description

The Xilinx® Defense-grade UltraScale™ high-performance FPGA family addresses a vast spectrum of system requirements with a focus on lowering total power consumption through numerous innovative technological advancements.

Defense-grade Kintex® UltraScale FPGAs: High-performance FPGAs with a focus on price/performance, using both monolithic and next-generation stacked silicon interconnect (SSI) technology. High DSP and block RAM-to-logic ratios and next-generation transceivers, combined with low-cost packaging, enable an optimum blend of capability and cost.

Defense-grade Virtex® UltraScale FPGAs: The industry's most capable high-performance FPGAs enabled using both monolithic and next-generation SSI technology to achieve the highest system capacity, bandwidth, and performance. Variants of the Virtex UltraScale family are optimized to address key market and application requirements through integration of various system-level functions, delivering unprecedented embedded memory and serial connectivity capabilities.

A long history of partnering with military agencies and the defense industry has resulted in Xilinx pioneering numerous advancements for Defense-grade reliability and security over four generations of devices.

Key Defense-grade features include:

- Full range extended temperature testing
- Mask set control
- Full compliance with MIL-PRF-38535 Pb content standards
- Longer-term availability
- Anti-counterfeiting features
- Ruggedized packaging
- Available information assurance (IA) methodology
- Available anti-tamper (AT) technology

Defense-Grade Family Comparisons

Table 1: **Defense-Grade Device Resources**

	Kintex UltraScale	Virtex UltraScale
System Logic Cells (K)	530–1,451	783–1,176
Block Memory (Mb)	21.1–75.9	44.3–60.8
DSP (Slices)	1,920–5,520	600–768
DSP Performance (GMAC/s)	7,297	1,015
Transceivers	8–64	40–64
Max. Transceiver Speed (Gb/s)	16.3	28.2
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	3,610
Integrated Blocks for PCIe®	3–6	2–4
Memory Interface Performance (Mb/s)	2,400	2,400
I/O Pins	520–728	520-702
I/O Voltage (V)	1.0–3.3	1.0–3.3

© Copyright 2017 Xilinx, Inc., Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, UltraScale, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. AMBA, AMBA Designer, ARM, ARM1176JZ-S, CoreSight, Cortex, and PrimeCell are trademarks of ARM in the EU and other countries. PCI, PCIe, and PCI Express are trademarks of PCI-SIG and used under license. All other trademarks are the property of their respective owners.

Summary of Features

I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken

Data is transported on and off chip through a combination of the high-performance parallel SelectIO™ interface and high-speed serial transceiver connectivity. I/O blocks provide support for cutting-edge memory interface and network protocols through flexible I/O standard and voltage support. The serial transceivers in the UltraScale devices transfer data up to 28.2Gb/s, enabling 25G+ backplane designs with dramatically lower power per bit than previous generation transceivers. All transceivers support the required data rates for PCIe Gen3, and Gen4 (rev 0.5), and integrated blocks for PCIe enable UltraScale devices to support up to Gen4 x8 and Gen3 x16 Endpoint and Root Port designs. Integrated blocks for 150Gb/s Interlaken and 100Gb/s Ethernet (100G MAC/PCS) extend the capabilities of UltraScale devices, enabling simple, reliable support for Nx100G switch and bridge applications.

Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as Hybrid Memory Cube (HMC).

Routing, SSI, Logic, Storage, and Signal Processing

Configurable Logic Blocks (CLBs) containing 6-input look-up tables (LUTs) and flip-flops, DSP slices with 27x18 multipliers, 36Kb block RAMs with built-in FIFO and ECC support are all connected with an abundance of high-performance, low-latency interconnect. In addition to logical functions, the CLB provides shift register, multiplexer, and carry logic functionality as well as the ability to configure the LUTs as distributed memory to complement the highly capable and configurable block RAMs. The DSP slice, with its 96-bit-wide XOR functionality, 27-bit pre-adder, and 30-bit A input, performs numerous independent functions including multiply accumulate, multiply add, and pattern detect. In addition to the device interconnect, in devices using SSI technology, signals can cross between super-logic regions (SLRs) using dedicated, low-latency interface tiles. These combined routing resources enable easy support for next-generation bus data widths.

Configuration, Encryption, and System Monitoring

The configuration and encryption block performs numerous device-level functions critical to the successful operation of the FPGA. This high-performance configuration block enables device configuration from external media through various protocols, including PCIe, often with no requirement to use multi-function I/O pins during configuration. The configuration block also provides 256-bit AES-GCM decryption capability at the same performance as unencrypted configuration. Differential power analysis (DPA) is a side-channel technique that observes and records samples of the power supply fluctuations due to digital switching (by monitoring voltage across a low resistance in series with the power line(s) or nearby electromagnetic probing) of a functioning electronic device. Signal processing and statistical methods can then be applied to the recorded data to extract red key data. Xilinx UltraScale devices provide DPA resistance by limiting the amount of side channel data that an adversary can collect

on any one key. For more information on DPA resistance see *Developing Tamper-Resistant Designs with UltraScale FPGAs Application Note* (XAPP1098). Additional features include SEU detection and correction, partial reconfiguration support, and battery-backed RAM or eFUSE technology for AES key storage to provide additional security. System Monitor enables the monitoring of the physical environment via on-chip temperature and supply sensors and can also monitor up to 17 external analog inputs.

The Defense Grade Kintex and Virtex devices are supported by the Xilinx Security Monitor 4.0 IP Core. *Integration and Verification of Security Monitor 4.0 for Kintex and Virtex UltraScale FPGAs* (XAPP1281) can be downloaded from the Xilinx security developers site (https://www.xilinx.com/member/design_security.html).

Full Range Extended Temperature Testing

Defense Grade FPGA products are offered in Military (M), Extended (E) and Industrial (I) temperature grades:

- Military: -55°C to +125°C
- Extended: 0°C to +100°C
- Industrial: -40°C to +100°C

Full range extended temperature testing includes full functional and parametric testing at room temperature plus hot and cold temperature extremes. Xilinx tests 100% of all die at wafer sort and 100% of all devices at Final Production testing. Xilinx continuously improves the test coverage of its products by implementing various design for test (DFT) methods that span digital logic, IP, memory elements, I/O boundary scanning, and many other areas. Xilinx test coverage improvements are achieving the highest test coverage possible, which are confirmed by PPM results from customer returns and are published on www.xilinx.com.

Mask Set Control

With Xilinx Defense-grade products, no mask changes are allowed. Because qualified mission critical applications cannot allow introduction of unknown factors, changes to the mask set used for device making might trigger a customer review and might require re-qualification of customer equipment. While commercial-grade devices can have changes for continuing yield improvement, Defense-grade products are exactly the same throughout the production life cycle.

Full Compliance with MIL-PRF-38535 Pb Content Standards

Xilinx Defense-grade products offer devices that are fully compliant to MIL-PRF-38535 with respect to Pb content in all solder interfaces and contain a minimum of 3% Pb. Many Aerospace and Defense applications require compliance to government flow downs where materials cannot contain more than 97% Tin (Sn). A risk for tin-whisker development exists where there is more than 97% tin. Components with solder terminals comprised of 3% Pb are not prone to tin whisker growth. In addition, the most commonly used lead-free solders are known to be more brittle than lead-tin solders, therefore in high vibration and shock applications, the ductile tin-lead solder joints are required.

Ruggedized Packaging

Ruggedized packages have a unique four-corner lid that has wider vent openings around the periphery. The lid used on Defense-grade RF/RL/RB/RS devices helps reduce the board-level cleaning processes needed prior to conformal coating. In the conformal coating process, boards go through a caustic material etch process to achieve the required conformal coating adherence. The selection of solvent cleaner (caustic material etch) or other corrosive chemicals can potentially cause issues with flip-chip packaging with smaller vent hole openings present for out-gassing of the organic materials used in the construction of flip-chip packaging. With the four-corner lid, much better cleaning and shorter manufacturing processes can be achieved, because the device can be fully flushed with the enhanced opening on the lid. Additional MIL-STD-883 group D specification stress tests are completed prior to production release of the defense grade (XQ) devices. The *Defense-Grade Kintex UltraScale and Virtex UltraScale Qualification Report* is available upon request.

MIL-STD-883 group D Qualification testing for Defense-grade products include the following:

- Physical dimensions (TM 2016)
- Thermal shock (TM 1011 condition B 15 cycles)
- Temperature cycling (TM 1010 condition C 100 cycles)
- Moisture Resistance (TM 1004)
- Vibration - Variable Frequency (TM 2007 Condition A minimum)
- Constant Acceleration - Centrifuge (TM 2001 Condition D minimum - Y1 orientation only)
- Salt Atmosphere (TM 1009 Condition A minimum)

Anti-counterfeiting Features

Xilinx Defense-grade devices offer multiple levels of anti-counterfeiting protection. Protection starts with the device package itself, since the unique four-corner lid construction differentiates it from the equivalent commercial device.

Having a different package makes the Defense-grade significantly more expensive for counterfeiters, who can no longer simply re-mark a commercial device and sell it as a Defense-grade product. Supplementing this is a unique laser marking, which uses micro watermarking characters and complex patterns that can be observed under low-power magnification.

Defense-Grade Kintex UltraScale FPGA Feature Summary

Table 2: **Defense-Grade Kintex UltraScale FPGA Feature Summary**

	XQKU040	XQKU060	XQKU095	XQKU115
System Logic Cells	530,250	725,550	1,176,000	1,451,100
CLB Flip-Flops	484,800	663,360	1,075,200	1,326,720
CLB LUTs	242,400	331,680	537,600	663,360
Maximum Distributed RAM (Mb)	7.0	9.1	4.7	18.3
Block RAM/FIFO w/ECC (36Kb)	600	1,080	1,680	2,160
Total Block RAM (Mb)	21.1	38.0	59.1	75.9
CMTs (1 MMCM, 2 PLLs)	10	12	16	24
I/O DLLs	40	48	64	64
Maximum HP I/Os[1]	416	520	650	624
Maximum HR I/Os[2]	104	104	52	104
DSP Slices	1,920	2,760	768	5,520
System Monitor	1	1	1	2
PCIe Gen3 x8	3	3	4	6
150G Interlaken	0	0	2	0
100G Ethernet	0	0	2	0
GTH 16.3Gb/s Transceivers[3]	20	32	32	64
GTY 16.3Gb/s Transceivers[4]	0	0	32	0

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in RS/RB packages support data rates up to 12.5Gb/s. See Table 3.
4. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s. See Table 3.

Defense-Grade Kintex UltraScale Device-Package Combinations and Maximum I/Os

Table 3: **Defense-Grade Kintex UltraScale Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)	Package Dimensions (mm)	XQKU040	XQKU060	XQKU095	XQKU115
		HR, HP GTH	HR, HP GTH	HR, HP GTH, GTY(4)	HR, HP GTH
RSA784(5)(6)	23x23	104, 364 8			
RBA676(5)	27x27	104, 208 16			
RFA1156	35x35	104, 416 20	104, 416 28	52, 468 20, 8	
RFA1517(6)	40x40		104, 520 32		
RLA1517(6)	40x40				104, 520 48
RLD1517	40x40				104, 234 64
RLF1924	45x45				104, 624 64
RFB2104(6)	47.5x47.5			52, 650 32, 32	
RLB2104(6)	47.5x47.5				104, 598 64

Notes:
1. Go to Defense-Grade UltraScale Ordering Information for package designation details.
2. RB/RF/RL packages have 1.0mm ball pitch. RS packages have 0.8mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., B2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
4. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s.
5. GTH transceivers in RS/RB packages support data rates up to 12.5Gb/s.
6. This product is not currently supported for designs in the Vivado Design Suite; for lead time and availability of this device-package combination, contact ad_marketing@xilinx.com.

Defense-Grade Virtex UltraScale FPGA Feature Summary

Table 4: **Defense-Grade Virtex UltraScale FPGA Feature Summary**

	XQVU065	XQVU095
System Logic Cells	783,300	1,176,000
CLB Flip-Flops	716,160	1,075,200
CLB LUTs	358,080	537,600
Maximum Distributed RAM (Mb)	4.8	4.8
Block RAM/FIFO w/ECC (36Kb each)	1,260	1,728
Total Block RAM (Mb)	44.3	60.8
CMT (1 MMCM, 2 PLLs)	10	16
I/O DLLs	40	64
Maximum HP I/Os(1)	468	650
Maximum HR I/Os(2)	52	52
DSP Slices	600	768
System Monitor	1	1
PCIe Gen3 x8	2	4
150G Interlaken	3	6
100G Ethernet	3	4
GTH 16.3Gb/s Transceivers	20	32
GTY 28.2Gb/s Transceivers	20	32

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Defense-Grade Virtex UltraScale Device-Package Combinations and Maximum I/Os

Table 5: **Defense-Grade Virtex UltraScale Device-Package Combinations and Maximum I/Os**

Package(1)(2)(3)	Package Dimensions (mm)	XQVU065	XQVU095
		HR, HP GTH, GTY	HR, HP GTH, GTY
RFC1517(4)	40x40	52, 468 20, 20	52, 468 20, 20
RFB2104(4)	47.5x47.5		52, 650 32, 32

Notes:
1. Go to Defense-Grade UltraScale Ordering Information for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., B2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
4. These device-package product combinations are not currently supported for designs in the Vivado Design Suite and will require additional qualification and testing to be completed prior to being made available for design and ordering. For lead time and availability of this device-package combination, contact ad_marketing@xilinx.com.

Device Layout

UltraScale devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. Figure 1 shows a device-level view with resources grouped together. For simplicity, certain resources such as the integrated blocks for PCIe, configuration logic, and System Monitor are not shown.

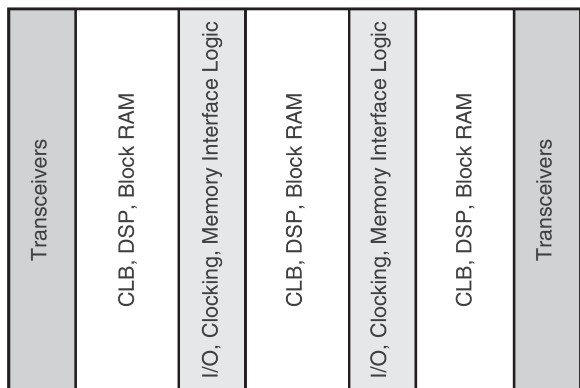

Figure 1: **FPGA with Columnar Resources**

Resources within the device are divided into segmented clock regions. The height of a clock region is 60 CLBs. A bank of 52 I/Os, 24 DSP slices, 12 block RAMs, or 4 transceiver channels also matches the height of a clock region. The width of a clock region is essentially the same in all cases, regardless of device size or the mix of resources in the region, enabling repeatable timing results. Each segmented clock region contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.

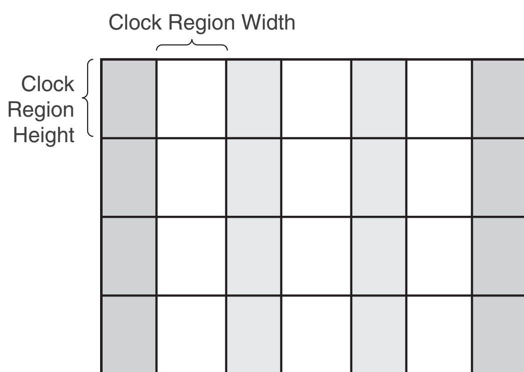

Figure 2: **Column-Based FPGA Divided into Clock Regions**

Input/Output

All UltraScale devices have I/O pins for communicating to external components.

The number of I/O pins in UltraScale FPGAs varies depending on device and package. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classified as high-range (HR) or high-performance (HP). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V.

All I/O pins are organized in banks, with 52 HP or HR pins per bank. Each bank has one common V_{CCO} output buffer power supply, which also powers certain input buffers. In addition, HR banks can be split into two half-banks, each with their own V_{CCO} supply. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). V_{REF} pins can be driven directly from the PCB or internally generated using the internal V_{REF} generator circuitry present in each bank.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100Gb/s and 400Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

GTH and GTY transceivers are used in the UltraScale FPGA architecture. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. Table 6 compares the available transceivers.

Table 6: **Transceiver Information**

	Kintex UltraScale		Virtex UltraScale	
Type	GTH	GTY	GTH	GTY
Quantity	8–64	0–32	20–32	20–32
Max. Data Rate	16.3Gb/s	16.3Gb/s	16.3Gb/s	28.2Gb/s
Min. Data Rate	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s
Applications	• Backplane • PCIe Gen4 • HMC	• Backplane • PCIe Gen4 • HMC	• Backplane • PCIe Gen4 • HMC	• 100G+ Optics • Chip-to-Chip • 25G+ Backplane • HMC

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally "auto-adapt" to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

Integrated Interface Blocks for PCI Express Designs

The UltraScale architecture includes integrated blocks for PCIe technology that can be configured as an Endpoint or Root Port. UltraScale devices are compliant to the PCI Express Base Specification Revision 3.0.

The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA.

This block is highly configurable to system design requirements and can operate up to the maximum lane widths and data rates listed in Table 7.

Table 7: **PCIe Maximum Configurations**

	Kintex UltraScale(1)	Virtex UltraScale(1)
Gen1 (2.5Gb/s)	x8	x8
Gen2 (5Gb/s)	x8	x8
Gen3 (8Gb/s)	x8	x8

Notes:

1. Transceivers in Kintex UltraScale and Virtex UltraScale devices are capable of operating at Gen4 data rates (16Gb/s).

For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed

transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCIe, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: link width and speed, maximum payload size, FPGA logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Integrated Block for Interlaken

Some UltraScale devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware time-stamping.

Clock Management

The clock generation and distribution components in UltraScale devices are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

Mixed-Mode Clock Manager

The mixed-mode clock manager (MMCM) can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

Three sets of programmable frequency dividers (D, M, and O) are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,600MHz, the phase-shift timing increment is 11.2ps.

PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

Clock Distribution

Clocks are distributed throughout UltraScale devices via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG_GT performs clock division from 1 to 8 for the transceiver clocks.

Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every UltraScale device includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, UltraScale FPGAs can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale devices support the highest bandwidth HMC configuration of 64 lanes with a single FPGA.

Configurable Logic Block

Every Configurable Logic Block (CLB) in the UltraScale architecture contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the UltraScale architecture have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They also have additional control signals to enable superior register packing, resulting in overall higher device utilization.

Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

Stacked Silicon Interconnect (SSI) Technology

Many challenges associated with creating high-capacity devices are addressed by Xilinx with the second generation of the pioneering 3D SSI technology. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with more than 17,000 low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs. Table 8 shows the number of SLRs in devices that use SSI technology and their dimensions.

Table 8: **UltraScale 3D IC SLR Count and Dimensions**

	Kintex UltraScale
Device	KU115
# SLRs	2
SLR Width (in regions)	6
SLR Height (in regions)	5

Block RAM

Every UltraScale device contains a number of 36Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. An additional pin on every block RAM controls the dynamic power gating feature.

Programmable Data Width

Each port can be configured as 32K × 1; 16K × 2; 8K × 4; 4K × 9 (or 8); 2K × 18 (or 16); 1K × 36 (or 32); or 512 × 72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from 16K × 1 to 512 × 36. Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36Kb FIFO or an 18Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27 × 18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors and external channels to the ADC.

All UltraScale architecture-based devices contain at least one System Monitor. See Table 9.

Table 9: **Key System Monitor Features**

	Kintex UltraScale Virtex UltraScale
ADC	10-bit 200kSPS
Interfaces	JTAG, I2C, DRP

FPGA sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

Configuration

UltraScale devices store their customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

UltraScale devices support secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the Kintex UltraScale and Virtex UltraScale families, go to UG570, *UltraScale Architecture Configuration User Guide*.

Xilinx UltraScale devices provide DPA resistance by limiting the amount of side channel data that an adversary can collect on any one key. For more information on DPA resistance see *Developing Tamper-Resistant Designs with UltraScale FPGAs Application Note* (XAPP1098).

UltraScale devices also have the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped. Designers can release their product with an early version of the design, thus getting their product to market faster. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in the field.

Configuring FPGAs

The SPI (serial NOR) interface (x1, x2, x4, and dual x4 modes) and the BPI (parallel NOR) interface (x8 and x16 modes) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself, eliminating the need for an external controller. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, x4, and dual x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide that are especially useful for processor-driven configuration are also supported by the FPGA. In addition, the new media configuration access port (MCAP) provides a direct connection between the integrated block for PCIe and the configuration logic to simplify configuration over PCIe.

Packaging

The UltraScale devices are available in a variety of organic flip-chip packages supporting different quantities of I/Os and transceivers. Maximum supported performance can depend on the style of package and its material. Always refer to the specific device data sheet for performance specifications by package type.

In flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

Defense-Grade UltraScale Ordering Information

Table 10 shows the speed and temperature grades available in the different device families.

Table 10: **Speed Grade and Temperature Grade**

Device Family	Devices	Speed Grade and Temperature Grade		
		Military (M)	Industrial (I)	Extended (E)
		–55°C to +125°C	–40°C to +100°C	0°C to +100°C
Kintex UltraScale	XQKU040 XQKU060 XQKU095	-1M (0.95V)	-2I (0.95V) -1I (0.95V)	-2E (0.95V)
	XQKU115			
Virtex UltraScale	XQVU065 XQVU095	-1M (0.95V)	-2I (0.95V) -1I (0.95V)	-2E (0.95V)

The ordering information shown in Figure 3 applies to all packages in the Kintex UltraScale and Virtex UltraScale FPGAs. Refer to the Package Marking section of UG575, *Kintex UltraScale and Virtex UltraScale FPGAs Packaging and Pinouts User Guide* for a more detailed explanation of the device markings.

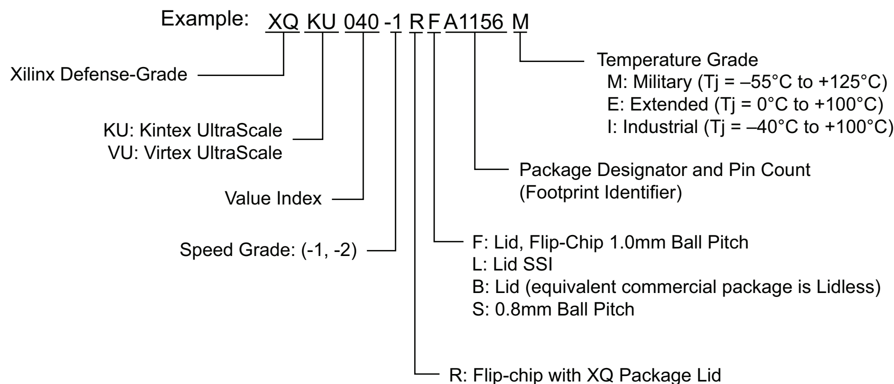

Figure 3: **Device Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
01/31/2017	1.0	Initial Xilinx release.

Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at http://www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at http://www.xilinx.com/ legal.htm#tos.

This document contains preliminary information and is subject to change without notice. Information provided herein relates to products and/or services not yet available for sale, and provided solely for information purposes and are not intended, or to be construed, as an offer for sale or an attempted commercialization of the products and/or services referred to herein.

Automotive Applications Disclaimer

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.